What is claimed is:

1. An image processing apparatus comprising:

a pixel matrix formation section consist of a device that has a rewritable circuit configuration, and having a plurality of line memories that output pixel data in parallel;

a filtering circuit consist of a device that has a rewritable circuit configuration, and performing filtering of pixel data by use of a pixel matrix based on the pixel data received in parallel from the line memories;

a memory for storing setting information for rewriting the configurations of the devices; and

a controller for rewriting the configuration of the line memories and the configuration of the filtering circuit by use of the setting information stored in the memory based on an image processing condition.

2. An image processing apparatus as claimed in Claim 1, wherein said image processing condition is the output image size.

3. An image processing apparatus as claimed in Claim 1, wherein said image processing condition the processing speed.

4. An image processing apparatus as claimed in Claim 1,

further comprising:

an operation panel for setting the image processing condition.

5. An image processing apparatus as claimed in Claim 4, wherein said controller rewrites the circuit configuration in accordance with the operation mode set with the operation panel.

6. An image processing apparatus as claimed in Claim 1, wherein said filtering circuit is used for image area determination.

7. An image processing apparatus as claimed in Claim 6, wherein the filtering circuit performs filtering for detecting an isolated point of an image.

8. An image processing apparatus comprising:

a processing circuit having a plurality of line memories and performing filtering of pixel data by use of a pixel matrix based on pixel data from the line memories;

a memory for storing setting information for rewriting the configuration of the processing circuit; and

a controller for rewriting the configuration of the line memories of the processing circuit and the configuration of

filtering by use of the setting information stored in the memory based on an image processing condition.

9. An image processing apparatus as claimed in Claim 8, wherein said image processing condition is the output image size.

10. An image processing apparatus as claimed in Claim 8, wherein said image processing condition the processing speed.

11. An image processing apparatus as claimed in Claim 8, further comprising:

an operation panel for setting the image processing condition.

12. An image processing apparatus as claimed in Claim 11, wherein said controller rewrites the circuit configuration in accordance with the operation mode set with the operation panel.

13. An image processing apparatus as claimed in Claim 8, wherein said processing circuit is used for image area determination.

14. An image processing apparatus as claimed in Claim 13, wherein the processing circuit performs filtering for detecting an isolated point of an image.

15. An image processing apparatus comprising:

a first circuit consist of a device that has a rewritable configuration, and having a plurality of line memories;

a second circuit for processing image data output from the line memories;

a memory for storing setting information for rewriting the configuration of the first circuit; and

a controller for rewriting the configuration of the line memories of the first circuit by use of the setting information stored in the memory based on an image processing condition.